Colocation of MEMS and Electronics

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This project bridges the gap between micro-electro-mechanical systems (MEMS) sensors and the necessary integrated circuits to communicate with and control/manipulate the MEMS. Since the advent of MEMS, electrical interconnections have been made using macroscopic wires to electrically bond the MEMS devices to integrated circuits for control and sensing. For a growing number of applications, the associated parasitic resistance and capacitance, as well as the large number of wires required, are not acceptable as an interconnect strategy. Several groups have produced MEMS devices and integrated circuits monolithically by fabricating the electronics next to the MEMS or using low temperature materials that can be deposited without exceeding the thermal budget of the integrated circuits. However, these strategies severely limit the types of MEMS devices that can be fabricated monolithically with integrated circuits. Further, for applications that require dense arrays of MEMS devices such as spatial light modulators (SLMs), packaging density is a vital metric. The area increase incurred by placing MEMS devices next to integrated circuits is not acceptable.

The technology to bond MEMS and integrated circuit dies together with microfabricated metal bumps will enable MEMS devices to be fabricated in conventional processes and then bonded to an integrated circuit.

Project Goals

This project established an enabling technology to colocate MEMS devices with integrated circuits. SLMs were used as the demonstration system since these systems benefit from both the scalability and the increased sensitivity of colocated integrated circuits. Arrays of micro-mirrors (for the SLM), as well as the corresponding high-voltage drivers were fabricated. The two dies were colocated by metal compression bonding. The resulting system was tested for mechanical and electrical functionality. An array of 25 micro-mirrors bonded to high-voltage drivers was assembled and tested.

Relevance to LLNL Mission

This project has relevance to a variety of LLNL interest areas. The ability to integrate MEMS devices and integrated circuits is an enabling technology within LLNL. This technology enables a new generation of devices for a wide variety of applications: chemical and biological sensors; targeting and tracking and location; biomedical devices; high-speed optical processing;

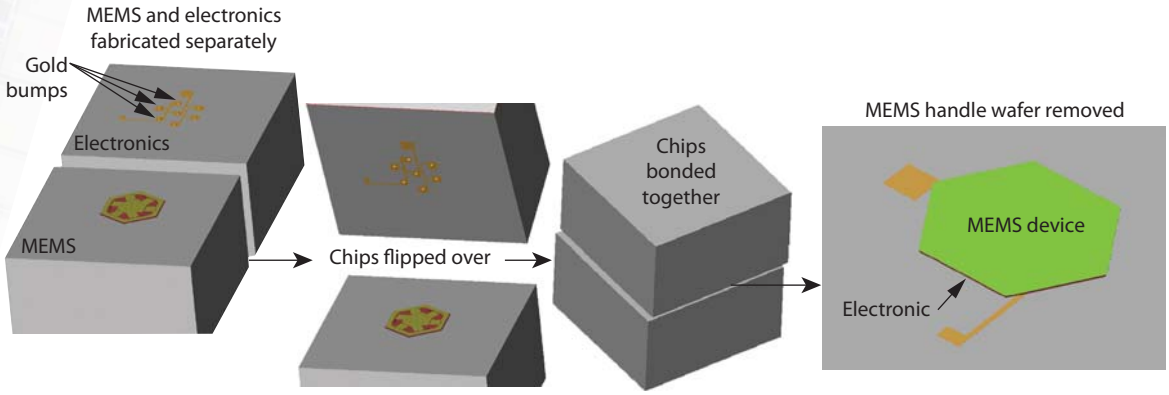

Figure 1. Schematic of overall process flow for the assembly of MEMS and integrated circuits.

and NIF target fabrication. This project has resulted in technology needed for the creation of meso- to microscale devices with nanoscale precision.

FY2006 Accomplishments and Results

In FY2006, the array of micro-mirrors and the high-voltage integrated circuits were fabricated and tested. Further, the micro-mirrors and integrated circuits were assembled and tested. Figures 1 to 3 illustrate our results. The details for each subtask are given below.

MEMS fabrication. The MEMS micro-mirrors were fabricated in the first quarter of FY2006. A large fraction of the fabrication process was carried out in LLNL's cleanroom. However, LPCVD deposition of polysilicon and silicon dioxide, which required well-characterized tools, was carried out at the UC Berkeley microfabrication facility. In the second quarter of FY2006, mechanical substitutes for the integrated circuit device were fabricated so the micro-mirror could be released and tested. The MEMS were released and tested in the third quarter of FY2006.

CMOS fabrication. We outsourced two integrated circuit fabrication runs in FY2006 based on plans completed in FY2005. The first two integrated circuit runs were shown to perform as predicted and work as expected, and a third CMOS run, which would have provided a backup in case one of the first two runs failed, was cancelled.

Assembly. A fabrication process for forming gold bumps for metal compression bonding was created with an external vendor. The MEMS micro-mirrors were then assembled to the integrated circuits by compression bonding the gold bumps against the corresponding metal pads on the integrated circuit die. The MEMS micro-mirrors were then separated from their substrate by breaking small silicon tethers.

Testing. The MEMS micro-mirrors were demonstrated to respond to electrostatic actuation on mechanical models of the integrated circuit die. The testing of the assembled device is ongoing.

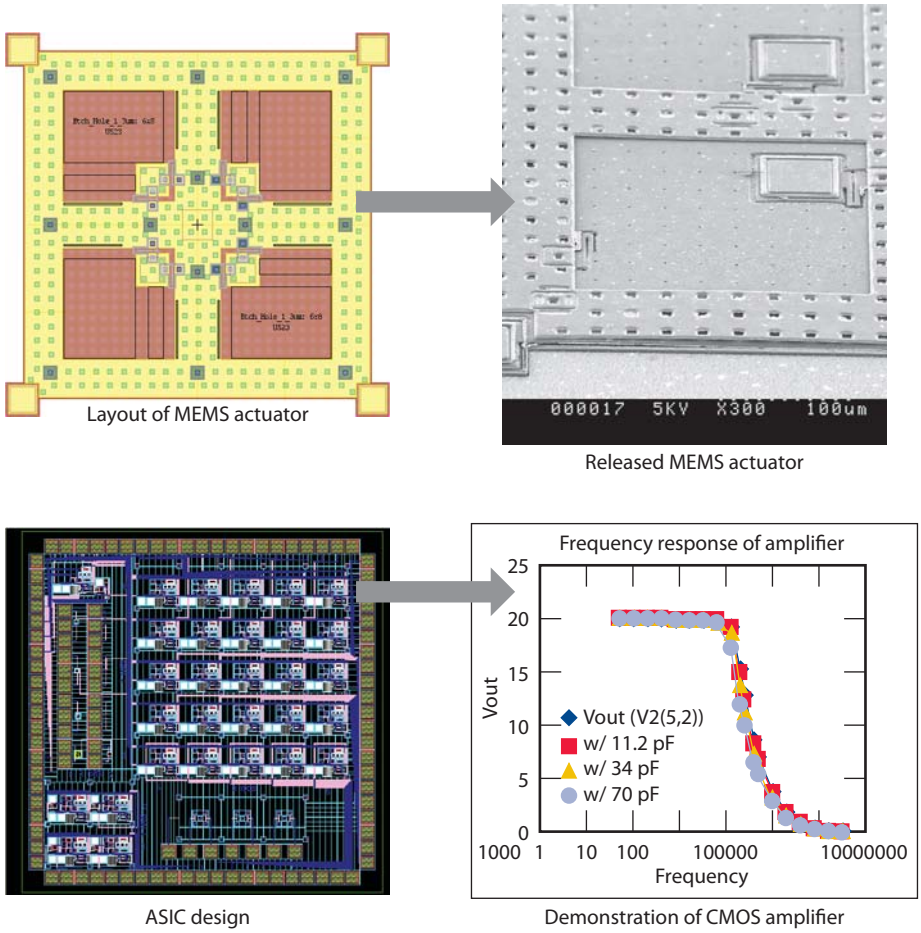

Figure 2. The schematics on the left side depict the layout of the MEMS micro-mirror and the integrated circuit. the images on the right side depict the fabricated micro-mirror and the measured frequency response of the integrated circuit.

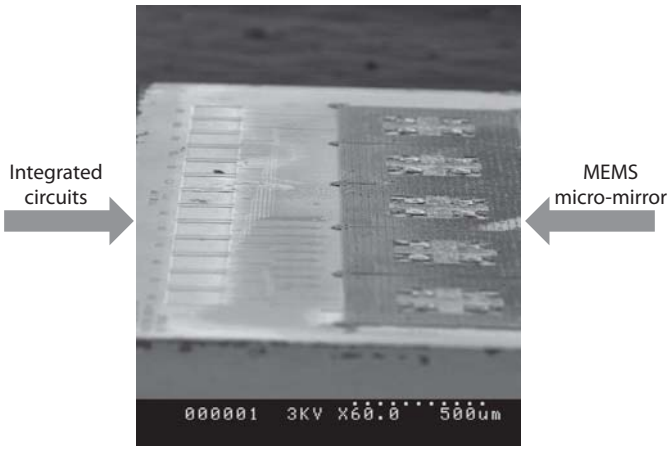

Figure 3. MEMs micro-mirrors colocated with integrated circuits.

Related References

1. Stappaerts E., "Differentially-Driven MEMS Spatial Light Modulator," U. S. Patent Number 6,791,735.

2. Singh, A., D. A. Horsley, M. B. Cohn, A. P. Pisano, and R. T. Howe, "Batch Transfer of Microstructures Using Flip-Chip Solder Bonding," *Journal of Microelectromechanical Systems*, **8,** 1, pp. 27-33, March 1999.

3. Humpston, G., and S. J. Baker, "Diffusion Bonding of Gold," *Gold Bulletin*, **31,** 4, 1998.